ABSTRACT

A system includes a first processor that performs a first self test process in response to a first actuation of a provided test control by a user of the system and a second processor that performs the second self test process in response to a second actuation of the test control prior to lapse of a first predefined period of time and terminates the second self test process in response to a third actuation of the test control by the user of the system, wherein the third actuation is maintained for more than a second predetermined period of time. In effect, a single test control formerly dedicated to a legacy processor is actuated to activate and control self testing of an additional processor.